

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No.09/652,550
Filing Date August 31, 2000
Inventor Keiji Jono et al.
Assignee Micron Technology, Inc.
Group Art Unit.....2811
Examiner Quang D. Vu
Attorney's Docket No. KM1-001
Title Methods of Forming an Isolation Trench in a Semiconductor,
Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods
of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor,
Trench Isolation Structures Formed in a Semiconductor, Memory Cells and
DRAMS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with
37 CFR §1.56. Copies of the cited art are included. No admission is made
regarding whether all the submitted references are prior art.

Respectfully submitted,

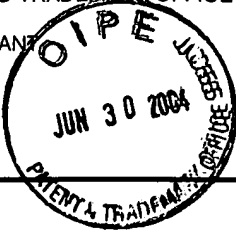
Dated: _____

6-30-04

By: _____

[Signature]
Mark S. Matkin
Reg. No. 32,268

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. KM1-001		SERIAL NO. 09/652,550	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT: Keiji Jono et al.			
				FILING DATE August 31, 2000		GROUP 2811	



U.S. PATENT DOCUMENTS							
*Examiner's Initials	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
AA	5,915,191	06/1999	Jun	438	431		
AB	6,087,705	07/2000	Gardner et al.	257	510		
AC	6,355,540 B1	03/2002	Wu	438	433		
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FOREIGN PATENT DOCUMENTS								
Document Number	Date	Country	Class	Subclass	Translation			
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AJ								
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)			
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EXAMINER		DATE CONSIDERED	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

EV 372458831



EL979953133

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/652,550
Filing Date August 31, 2000
Inventor Keiji Jono et al.
Assignee KMT Semiconductor, LTD and Micron Technology, Inc.
Group Art Unit 2811
Examiner Quang D. Vu
Attorney's Docket No. KM1-001
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods of
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DRAMS

COPY

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

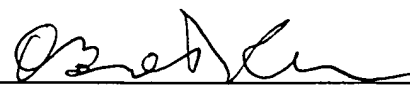
References -See Attached Form PTO-1449

The Examiner's attention is directed to the references which are listed on the attached Form PTO-1449, copies of which are attached. No admission is made regarding whether all the submitted references are prior art.

Citation of the referenced art is respectfully requested.

Respectfully submitted,

Dated: 2-2-04

By: 
D. Brent Kenady
Reg. No. 40,045

EV372458831

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
KM1-001SERIAL NO.
09/652,550LIST OF ART CITED BY APPLICANT
(Use several sheets if necessary)

APPLICANT: Keiji Jono et al.

FILING DATE
August 31, 2000GROUP
2811

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,081,662	06/27/00	Murakami et al.			
	AB	5,994,198	11/30/99	Hsu et al.			
	AC						
	AD						
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FOREIGN PATENT DOCUMENTS

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	AM							
	AN							
	AO							
	AP							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

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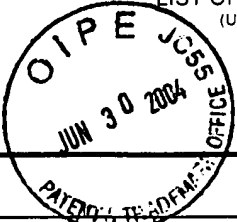
Respectfully submitted,

Dated: 3-10-03

By: 
D. Brent Kenady
Reg. No. 40,045

EV 372458831

EV 085427812

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. KM1-001		SERIAL NO. 09/652,550	
<div style="text-align: center;">  </div> <div style="text-align: center;"> LIST OF ART CITED BY APPLICANT <small>(Use several sheets if necessary)</small> </div>				APPLICANT: Keiji Jono et al.			
				FILING DATE August 31, 2000		GROUP 2811	
U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	6,034,409	03/07/2000	Sakai et al.			
	AB	6,171,924 B1	01/09/2001	Wang et al.			
	AC	6,154,417	11/28/2000	Kim			
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